EMBEDDED NETWORKED FRONT EN
BEYOND THE CRATE

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Outline

- Crates *vs.* Embedded Front Ends
- Examples of existing Embedded Front Ends
- How can we make Front Ends even better?

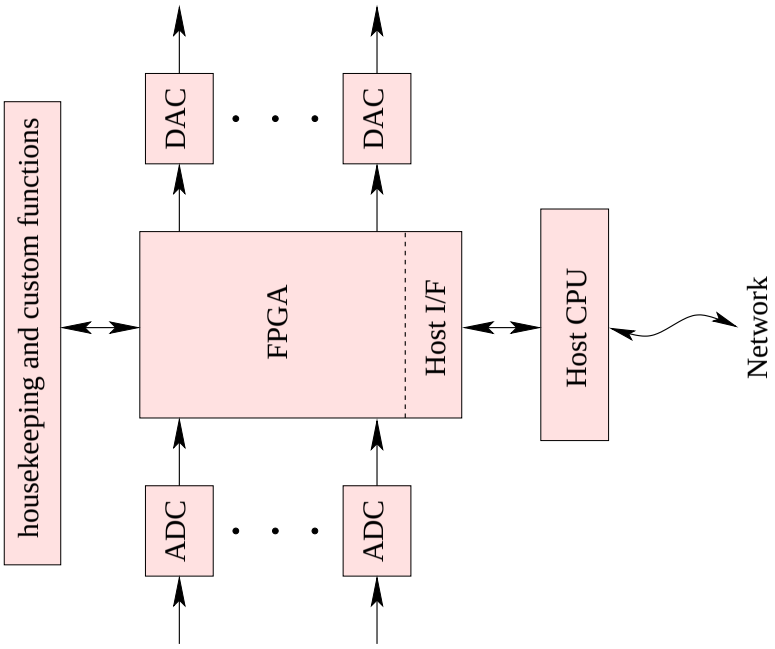
Crates

- Large and Inflexible
- Backplane data transfer slow, complex, high pin count
- Infrastructure provided is dated
  asynchronism → noise, metastability, complication
- High power → fans → noise, reliability concerns
- Switching power supplies → electrical noise
- Other people have a rosier assessment than this

Networked front end

- Single purpose: sensor/actuator bridged to network
- Fully integrated with accelerator (e.g., timing, interlocks)
  - No adapter/transition hardware needed
  - Field wiring becomes quieter and more maintainable
- Design patterns, schematics, software, and sometimes hardware reused

Taiwan block diagram



Housekeeping checklist

- Power supply monitoring
- FPGA core current draw
- Temperature
- Serial number

Usually implemented with serial communication: SPI, I^2C, 1-Wire

Ideally, all I/O monitored for correctness: shorts, opens, missing clocks, etc.

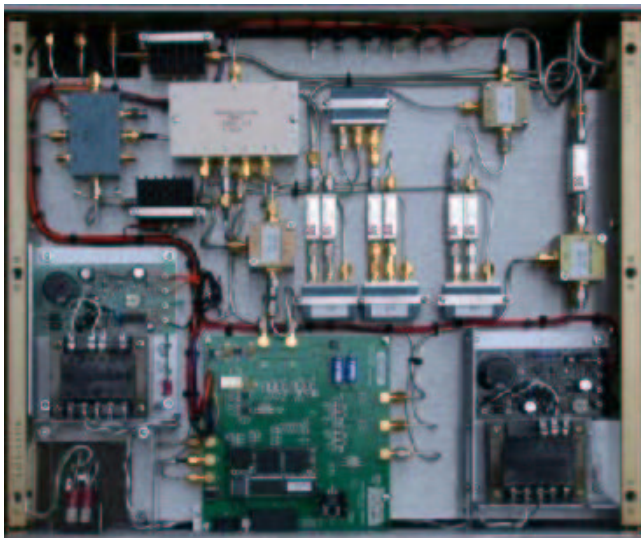
Computers

- multiple sources, very competitive market
- usually needs additional glue
- usually good throughput, but unpredictable latency
- widely understood, everybody thinks they know how to program one

FPGA

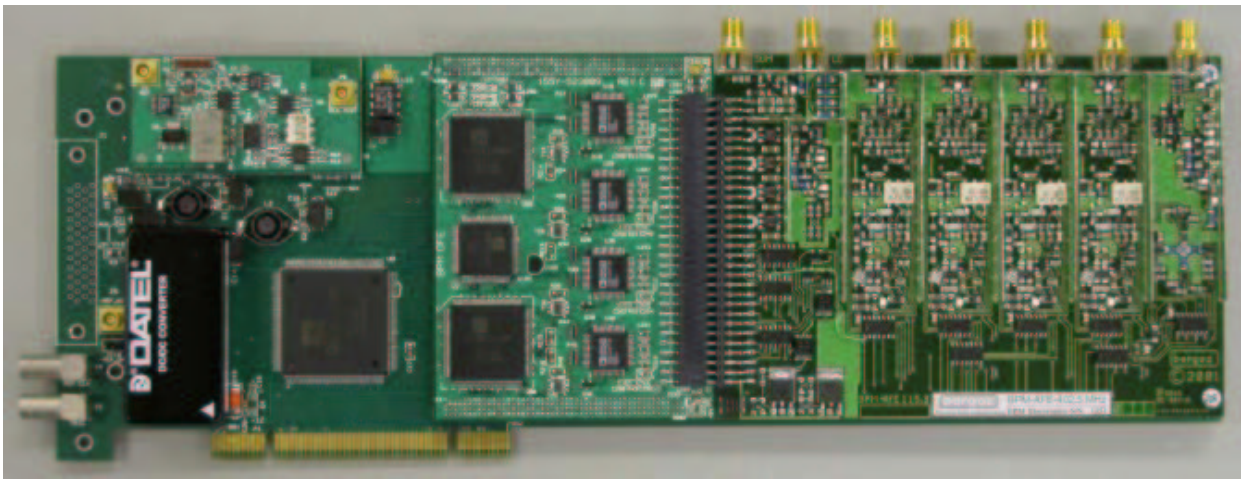
- chip design strongly protected by patents, two vendors dominate
- handles glue very well
- guaranteed latency normally designed-in
- reputation for being difficult to program

Accelerator Low Level RF control: SNS/LBNL Interim LLRF system



- connectorized RF plumbing
- 4 × 40MS/s 12-bit ADCs
- 12-bit 80 MS/s DAC
- Xilinx XC2S150 FPGA runs feedback within pulses
- plug-on 200 MIPS single board computer (nanoEngine)
- All linear power supplies to minimize electrical noise

Accelerator Beam Position Monitor readout: SNS/LANL BPM

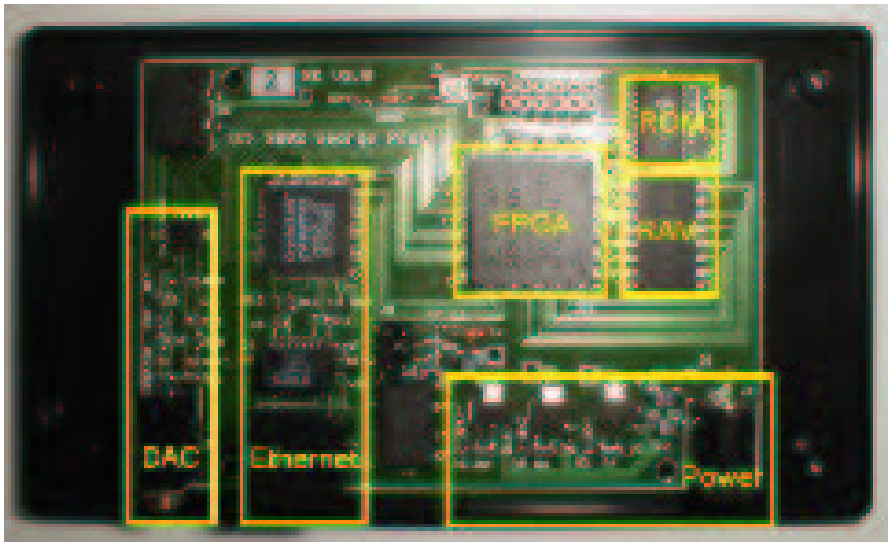


- Daughter card for RF downconversion
- 4 × 40MS/s 14-bit ADCs
- 8 × 256K deep FIFOs
- PCI bus form factor, within a commercial 1U rack-mounted PC chassis
- Quicklogic CPLD for PCI interface and custom logic.

Network Video Input: Elphel Model 303 Camera

- Xilinx XC2S300E FPGA compresses from raw pixels to JPEG format.
- ETRAX 32-bit CPU bridges data to Ethernet, at a sustained rate of 15 megapixels each) per second.
- Powered by 48VDC through the Ethernet cable (IEEE 802.3af).

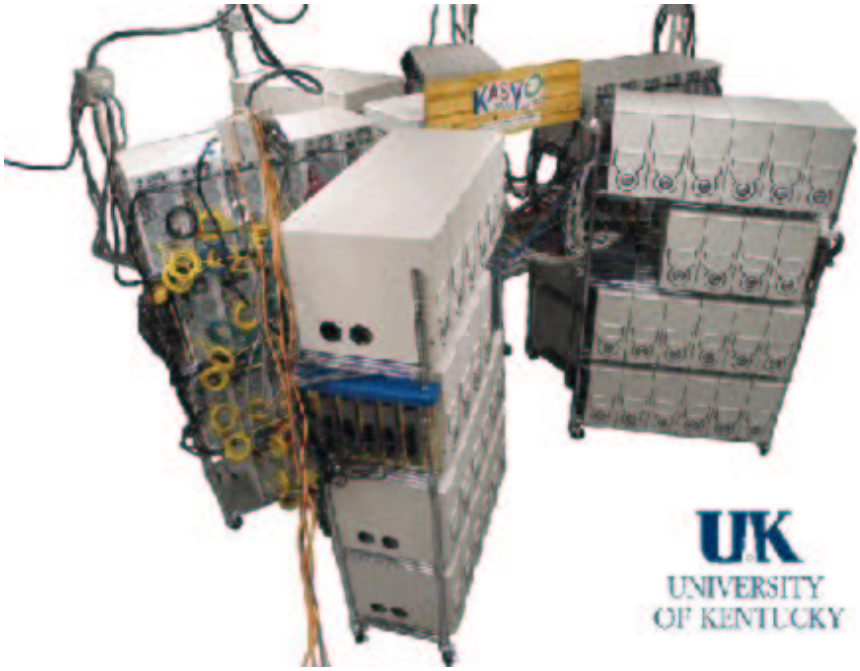
Network Audio output: LANPipe



- 16-bit CPU implemented on the XC2S30 FPGA
- CPU runs a simple UDP/IP network stack
- Ethernet chip includes both the PHY and MAC

Back End Implications

- Can the Global Control Sytem deal with needed network I/O? Yes!



- 128 2.0 GHz Athlons
- 400 GFLOPS for US$40000
- High bandwidth interconnect
- With more network gear, could accept traffic from up to 1408 Front Ends

Next step: merge FPGA and CPU

- Increase performance
- Reduce chip count (maybe)
- One less clock domain
- Hard core *vs.* soft core
- Inline *vs.* adjunct CPU

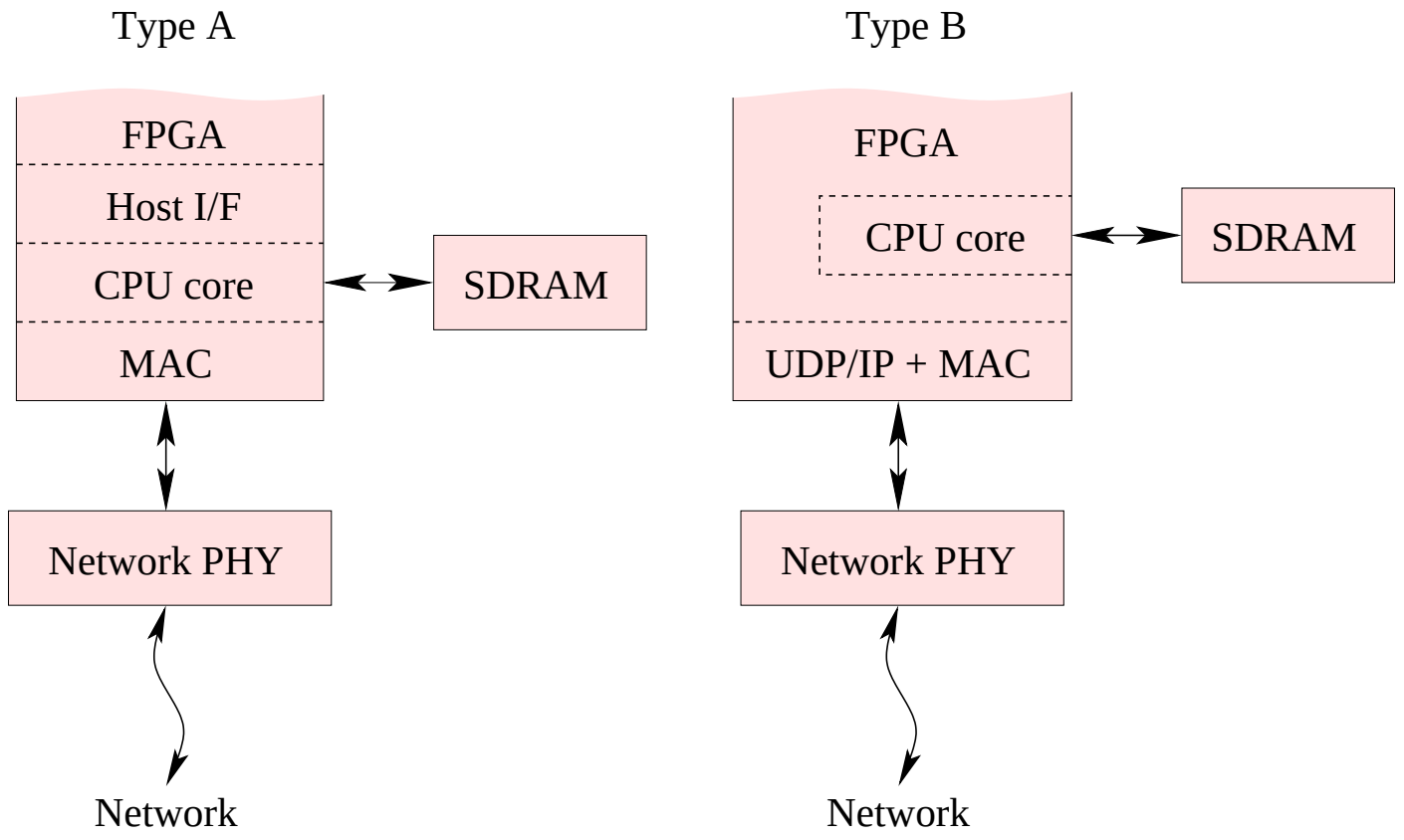
Soft Cores

name	source	bits	4-LUTs	MHz
PicoBlaze	VHDL	8	152	40
gr0040	Verilog	16	257	50
xr16	schem	16	392	65
MicroBlaze	N/A	32	1050	75
NIOS-16	N/A	16	1100	50
NIOS-32	N/A	32	1700	50
LEON SPARC	VHDL	32	4800	65
Aquarius	Verilog	32	5506	21
or1k	VHDL	32	6000	33

Hard Cores

CPU core	chip	bits	MHz
PowerPC	Xilinx Virtex-IIpro	32	250
ARM9	Altera Excalibur	32	200
80C51	Triscend	8	

How the CPU fits on the FPGA


Type A
FPGA
Host I/F
CPU core
MAC
SDRAM
Network PHY
Network
Type B
FPGA
CPU core
UDP/IP + MAC
SDRAM
Network PHY
Network

"The cheapest, fastest and most reliable components of a computer system ar
aren't there." - Gordon Moore, DEC

Upcoming issues

- Reliable and flexible booting
  - firmware/software upgrades over network
- Connecting performance and protocol
  - Wire speeds with stripped down protocol handled without a CPU
  - Corresponding driver/gateway on workstation/server end
- Demonstrate cooperation, portability, and maintenance of large FPGA co
- Intellectual property minefield
  - Find a way to build on solid, publicly owned foundations
- Old joke: What's the difference between hardware and software?

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- Intellectual property minefield
  - Find a way to build on solid, publicly owned foundations
- Old joke: What's the difference between hardware and software?
  - Hardware keeps getting cheaper, faster, and smaller!

Conclusions

Great promise for distributed control and acquisition, especially once you crate.